REMARKS

Claims 1, 3, 4, 5 and 16-19 are pending in the application.

Claims 6-15 were previously cancelled without prejudice or disclaimer to the subject matter contained therein.

Claim 2 is cancelled without prejudice to the subject matter contained therein.

Claims 1, 4, 16, 18 and 19 are amended for "clarification purposes" and no new matter is added or issues raised.

I. Claim Rejections - 35 U.S.C. §102

The rejection of claims 1, 3-5 and 16-19 under 35 U.S.C. § 102(b) as being anticipated by Richter (USP 5,623,490) is traversed.

In applicant's invention, a data packet processor includes a scheduler that assigns priority information to each received data packet. The priority information determines an order of the data packets to be processed. The processor also includes an external memory, an internal memory and a memory manager.

The memory manager transfers one or more packets with high priority and which are stored in the external memory into the internal memory. Thus, in applicant's invention, data packets having the highest priority of all received data packets are transferred to the internal memory by the memory manager to be processed as one of the next. It is the memory manager that also transfers packets from the internal memory back to the external memory.

In Richter, referring to Figs. 7A and 7B, and to col. 7 lines 31-52, blocks 708-712 generate packets with priority. Block 714 arranges the packets according to their priority

and places the packets in the write WriteQueue 716 in their order of priority. From 716 the packets are sent to either read queue 722 or 724, depending on the identity of the caller. Assuming that the caller is CALLER 2, the packets in read queue 722, which is a buffer memory for storing packets, are forwarded to control means 726, which selects and processes the packets according to their priority. From the above it is clear that Richter neither discloses nor suggests the structure now positively recited in claim 1, that being, in combination, the structure of an external memory, an internal memory, and a memory manager coupled to both the external memory and the internal memory where it is the memory manager which transfers those packets which are to be processed next from the external memory to the internal memory, and where the memory manager is operable to transfer a data packet from the internal memory back to the external memory.

Claim 1 now recites, in combination, the structure of,

"A data packet processing device for processing data packets received from a network, including ...

a scheduler for assigning priority ... to each received data packet in the external memory ...

an internal memory for storing data packets;

a memory manager coupled to the external memory and the internal memory operable to transfer the data packet having the highest priority stored in the external memory to the internal memory to be processed as one of the next;

wherein the memory manger is operable to transfer a data packet from the internal memory to the external memory" (underscoring added for emphases).

Nowhere does Richter disclose or even suggest the structure that is now positively recited in claim 1, that of a memory manager coupled to both the external and internal memories and operatively transfers only packets with high priority which are to be processed as one of the next from the external buffer to the internal buffer, and where the memory manager is operable to transfer a data packet from the internal buffer back to the external buffer. For the reasons noted, it is our understanding that claim 1 clearly avoids Richter and is in condition for allowance. Claims 3, 4 and 5 depend from claim 1 and, therefore, are also considered to be in condition for allowance.

Amended claim 16 now recites,

"A method for processing a data packets, said method comprising...

storing the data packets in an external memory;

determining a priority of the received data packet and assigning priority information to each of the data packet..."

in combination with

"...transferring at least one of the packets having the highest priority to an internal memory for storage and processing as one of the next data packets;

transferring a data packet from the internal memory to the external memory if the priority information indicates that the priority of the data packet is not high; and

storing a pointer link to the data packet in a pointer memory to facilitate

processing in the data packet's assigned priority order". (underscoring added for emphases).

Clearly, Richter neither discloses nor suggests transferring a packet having the high priority from the external memory to the internal memory for storage and processing, in combination with, transferring a packet having a low priority from the internal memory to the external memory. For this reason it is understood that claim 16 is in condition for allowance. Claim 17 depends from claim 16 and is also in condition for allowance.

For the reason noted above for claim 16, independent claims 18 and 19 are also considered to be in condition for allowance.

CONCLUSION

In view of the above, each of the presently pending claims in this application is believed to be in condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

The Examiner is respectfully requested to contact the undersigned at the telephone number indicated below if the Examiner believes any issue can be resolved through either a Supplemental response or an Examiner's Amendment.

Respectfully submitted,

Steven Fischman
Registration No. 34,594

SCULLY, SCOTT, MURPHY & PRESSER, P.C.
400 Garden City Plaza, Suite 300
Garden City, New York 11530
(516) 742-4343
SF/EW/ech